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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

E

Office Action Summary	Application No.	Applicant(s)	
	10/664,055	BARRETT ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2003 and 17 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Specification and Drawings as received on 17 September 2003; Oath and Declaration 14 June 2004 and 14 August 2003; Extension of Time for Two Months as received 15 June 2004; Petition as received on 12 July 2004; and Power of Attorney as received on 17 June 2005.

Specification

3. The disclosure is objected to because of the following informalities:

   a. Page 20, lines 29-30 recites "FIG. 4 shows a flow chart representing a method of processing an instruction in an instruction pipeline..." However, the Figure 4 in the drawings is not a flow chart but an apparatus drawing showing the stages of the pipeline and how the invention determines if an interrupt is present within the device.

   b. Page 20, line 37 and page 21, lines 5 and 7 disclose a "de-multiplexer". However, the drawings (Figure 4, element 6) shows a multiplexer. A "de-multiplexer", by conventional definitions, is the converse of a multiplexer, which receives multiple inputs and has a single output, so a "de-multiplexer" is receives an input and has multiple outputs. Please see the accompanying definitions from Heuring et al. and Ken Bigelow.

4. Appropriate correction is required.

Drawings

5. A new corrected drawing for Figure 4 in compliance with 37 CFR 1.121(d) is required in this application because Figure 4 is mainly a hand drawn drawing with typed words. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 3 and 6-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 3 recites the limitation "the instruction fetch stage" in line 3. There is insufficient antecedent basis for this limitation in the claim. Claim 3 depends from claim 1, which also does not previously establish an instruction fetch stage. Also, claim 3 is almost claim 1, limitation (b) verbatim except for "the instruction fetch stage" language. It is unclear whether the claim is meant to modify claim 1, limitation (b) by stating which stage the instruction being replaced is in or whether it is an entirely separate claim limitation that is to be added.

9. Claim 6 recites the limitations "the information of the program counter" and "the sort of interrupt" in lines 2 and 3. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 7 recites the limitations "the data content of a program counter" and "the data content of an interrupt" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

11. Claim 8 recites the limitations "the program counter", "the sort of interrupt", and "the actual instruction" in lines 4, 5, and 7. There is insufficient antecedent basis for this limitation in the claim.

12. Claim 9 recites the limitations "the instruction fetch" and "the second input" in lines 3 and 4. There is insufficient antecedent basis for this limitation in the claim.

13. Claim 11 and 13 recite the limitations "the data content of the program counter" and "the data content of the interrupt register" in lines 2 and 3. There is insufficient antecedent basis for this limitation in the claim.

14. Claim 12 recites the limitations "the output of the comparator", "the first input of an or-operator", "the second input of the or-operator", "the signal received from the interrupt controller", and "the signal received from the comparator" in lines 2-5. There is insufficient antecedent basis for this limitation in the claim.

15. Claim 15 recites the limitations "the instruction coming from the output of the de-multiplexer" and "the instruction pipeline of the processor" in lines 2 and 3. There is insufficient antecedent basis for this limitation in the claim.

16. Claim 16 recites the limitation "the instruction pipeline of the processor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

17. Claim 17 has the limitation "the interrupt". However, it is unclear which interrupt is being referred to by this language: the external interrupt or the interrupt pseudo-instruction.

Also, claim 17 recites the limitation "the instruction state stages" in line 2. There is insufficient antecedent basis for this limitation in the claim.

18. Claim 18 recites the limitation "the interrupt request" in line 3-4. There is insufficient antecedent basis for this limitation in the claim. Also, claim 18 has the limitations "the instruction". However, it is unclear which interrupt is being referred to by this language: the actual instruction or the interrupt pseudo-instruction.

19. Claim 19 recites the limitations "the interrupt request" and "the instruction fetch stage" in lines 3-5. There is insufficient antecedent basis for this limitation in the claim.

20. Claim 20 recites the limitation "the co-processor" in line 3. There is insufficient antecedent basis for this limitation in the claim.

21. Referring to claims 9-17, where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "de-multiplexer" in claim9 is used by the claim to mean a multiplexer, which "connects a number of inputs to a single output", while the accepted meaning is "the converse of a MUX", which is a connection with an input to a number of outputs. The term is indefinite because the specification does not clearly redefine the term. Please see the accompanying definitions from Heuring et al. and Ken Bigelow.

Claim Rejections - 35 USC § 102

22. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

23. Claims 1-3, 5-7, and 24 are rejected under 35 U.S.C. 102(b) as being taught by Case et al., U.S. Patent Number 4,777,587 (herein referred to as Case).

24. Referring to claims 1 and 24, taking claim 1 as exemplary, Case has taught a method of processing an interrupt verification support mechanism in a computer system comprising a processor and an input for external interrupts communicatively coupled to the processor (Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B), the method comprising the steps:

a. Processing at least one actual instruction in the processor (Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B); and

b. If an external interrupt request or an interrupt pseudo-instruction is received by the processor, the actual instruction is replaced with the pseudo-instruction (Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B).

25. Claim 24 is substantially similar in limitations to claim 1 and is rejected for the reasons above. The only difference is that claim 24 is a computer utilizing the method recited in claim 1.

26. Referring to claim 2, Case has taught processing at least one actual instruction in the

processor in an instruction pipeline wherein instructions are processed concurrently by an instruction fetch stage, an instruction decode stage, an instruction issue stage, an instruction execute stage and a result write-back stage (Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B). In regards to Case, the fetch stage and issue stage functions are both found in Case's fetch stage, since it both fetches the instruction from the cache based upon the instruction address in the PC issued by the MUX (Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B).

27. Referring to claim 3, Case has taught if an external interrupt request or an interrupt pseudo-instruction is received by the processor, replacing the actual instruction present in the instruction fetch stage with the pseudo-instruction (Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B).

28. Referring to claim 5, Case has taught simultaneously processing a number of instructions in the processor in an instruction pipeline with several instruction stages each instruction being in a different instruction stage at a time (Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B).

29. Referring to claim 6, Case has taught storing at least the information of the program counter of the instruction which is to be interrupted and the sort of interrupt to use in a set of one or more interrupt registers of the processor (Case column 1, lines 42-50; column 2, lines 47-59;

column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B).

30. Referring to claim 7, Case has taught comparing the data content of a program counter with the data content of an interrupt register and replacing the actual instruction with a pseudo-instruction when the data content of the program counter matches the data content of the interrupt register, or when an external interrupt is present (Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B).

Claim Rejections - 35 USC § 103

31. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

32. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Case et al., U.S. Patent Number 4,777,587 (herein referred to as Case) as applied to claim 1 above, in view of Sproul, III, U.S. Patent Number 4,498,136 (herein referred to as Sproul). Case has not taught creating the pseudo-instruction by a co-processor connected to the processor. Sproul has taught creating the pseudo-instruction by a co-processor connected to the processor (Sproul Abstract; column 4, lines 16-37; and Figure 2). In regards to Sproul, the device disclosed is a separate interrupt processor to assist with interrupt decoding and handling. A person of ordinary skill in the art at the time the invention was made, and as taught by Sproul, would have recognized that the interrupt co-processor of Sproul improves interrupt management in a pipeline (Sproul column

3, lines 10-23). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the interrupt co-processor methods of Sproul in the device of Case to improve interrupt handling in a pipelined system.

33. Claims 8-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Case et al., U.S. Patent Number 4,777,587 (herein referred to as Case) in view of Sproul, III, U.S. Patent Number 4,498,136 (herein referred to as Sproul).

34. Referring to claims 8 and 23, taking claim 8 as exemplary, Case has taught an interrupt verification support mechanism device for a computer system comprising

a. A processor and an input for external interrupt requests or interrupt pseudo-instructions communicatively coupled to the processor (Case column 1, lines 42-50; column 2, lines 47-59; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B),

b. Wherein the device includes at least the program counter of the instruction which is to be interrupted and the sort of interrupt to use, so as to enable the device to process at least one actual instruction (Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B), and

c. If an external interrupt request is received by the processor, the actual instruction is replaced with the pseudo-instruction (Case column 1, lines 42-50; column 2, lines 47-59; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B).

35. Case has not explicitly taught a set of one or more interrupt registers each of which contains information. However, Case has taught that the PC addresses of the instructions flushed from the pipeline must be saved (Case column 1, lines 42-50; column 2, lines 47-59; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B). Sproul has taught a set of one or more interrupt registers each of which contains information (Sproul Abstract; column 4, lines 16-37; and Figure 2). In regards to Sproul, the device disclosed is a separate interrupt processor to assist with interrupt decoding and handling. A person of ordinary skill in the art at the time the invention was made, and as taught by Sproul, would have recognized that the interrupt co-processor of Sproul improves interrupt management in a pipeline (Sproul column 3, lines 10-23). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the interrupt co-processor methods of Sproul in the device of Case to improve interrupt handling in a pipelined system.

36. Claim 23 is substantially similar in limitations to claim 8 and is rejected for the reasons above. The only difference is that claim 23 is a computer comprising the device of claim 8.

37. Referring to claim 9, Case in view of Sproul has taught wherein the device further comprises an instruction fetch with a program counter and an interrupt register (Sproul Abstract; column 4, lines 16-37; and Figure 2), the instruction fetch being coupled to a first input of a de-multiplexer for transmitting instructions to said de-multiplexer, the second input of the de-multiplexer connected to an interrupt pseudo-instruction input and the program counter connected with the interrupt register by a comparator (Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B).

38. Referring to claim 10, Case in view of Sproul has taught wherein the second input of the de-multiplexer is capable of receiving interrupt pseudo-instruction signals or external interrupt requests (Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B).

39. Referring to claim 11, Case in view of Sproul has taught wherein the comparator creates a high level signal only if the data content of the program counter matches the data content of the interrupt register (Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B).

40. Referring to claim 12, Case in view of Sproul has taught wherein the output of the comparator is connected to the first input of an or-operator and the second input of the or-operator is connected to an interrupt controller so as to enable the or-operator to create a high level signal if the signal received from the interrupt controller differs from the signal received from the comparator (Sproul Abstract; column 4, lines 16-37; and Figure 2).

41. Referring to claim 13, Case in view of Sproul has taught wherein, when the data content of the program counter matches the data content of the interrupt register, the actual instruction is replaced with a pseudo-instruction (Case column 1, lines 42-50; column 2, lines 47-59; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B)

42. Referring to claim 14, Case in view of Sproul has taught wherein when an external interrupt request is present at the de-multiplexer, the actual instruction is replaced with an interrupt pseudo-instruction (Case column 1, lines 42-50; column 2, lines 47-59; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B).

43. Referring to claim 15, Case in view of Sproul has taught wherein the instruction coming from the output of the de-multiplexer is sequentially processed in the instruction pipeline of the processor (Case column 1, lines 42-50; column 2, lines 47-59; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B).

44. Referring to claim 16, Case in view of Sproul has taught wherein the instruction pipeline of the processor includes an instruction fetch stage, an instruction decode stage, an instruction issue stage, an instruction execute stage and a result write-back stage (Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B). In regards to Case, the fetch stage and issue stage functions are both found in Case's fetch stage, since it both fetches the instruction from the cache based upon the instruction address in the PC issued by the MUX (Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B).

45. Referring to claim 17, Case in view of Sproul has taught wherein the interrupt pseudo-instruction effects the instruction state stages required by the interrupt (Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B).

46. Referring to claim 18, Case in view of Sproul has taught wherein if an interrupt request or an interrupt pseudo-instruction is received by the processor, the processor is adapted to cancel an instruction that is in the instruction fetch stage when the interrupt request or the interrupt pseudo-instruction is received and to reissue the instruction starting at the instruction fetch stage

(Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B).

47. Referring to claim 19, Case in view of Sproul has taught wherein if an interrupt request or an interrupt pseudo-instruction is received by the processor, the processor is adapted to cancel an instruction that is in any instruction stage when the interrupt request or the interrupt pseudo-instruction is received and to reissue the instruction starting at the instruction fetch stage (Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B).

48. Referring to claim 20, Case in view of Sproul has taught wherein the pseudo-instruction is created by a co-processor connected to the processor (Sproul Abstract; column 4, lines 16-37; and Figure 2). In regards to Sproul, the device disclosed is a separate interrupt processor to assist with interrupt decoding and handling.

49. Referring to claim 21, Case in view of Sproul has taught wherein the device is a media decoding system, the processor is a core decoder processor (Case column 1, lines 42-50; column 2, lines 47-59; column 2, line 26 to column 3, line 63; Figure 1; column 5, line 24 to column 6, line 44; and Figures 3A and 3B) and the co-processor is a decoding accelerator adapted to assist the core processor with a decoding function (Sproul Abstract; column 4, lines 16-37; and Figure 2).

50. Referring to claim 22, Case in view of Sproul has taught wherein the processor is a reduced instruction set computer (RISC) processor (Case column 1, lines 15-19).

Conclusion

51. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Davis et al., U.S. Patent Number 4,755,935, has taught a jump handling method that includes handling interrupts.

b. Crump et al., U.S. Patent Number 5,557,759, has taught an interrupt handling device in a media processor.

52. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

53. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

54. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
06 April 2006

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